REGIONAL RELIABILITY STUDIES USING A MULTI-AREA PROGRAM

An engineer’s perspective on system reliability varies depending on his objective. The engineer concerned with planning a large interconnected system needs to take a macroscopic view of load and generation in several “areas.” He is concerned with reserve requirements of each area and with the exploitation of capacity and load diversity. He must treat inter-area transfer capability as an aggregate quality of the interconnection.

However, to the engineer concerned with detailed configuration of a system or substation, reliability requires something else. He has to worry about the risk of interruption of loads and the severity of individual equipment or line overloads. The microscopic aspect of system reliability means getting down to detail on individual generator and circuit outage rates and the effects of alternative system and substation configurations on the quality of service.

This article addresses the first of these two tasks. An article prepared for the next issue of the PTI Newsletter will discuss the second. Both will describe newly-developed or recently-enhanced PTI computer programs for the objectives cited.

Interconnections of neighboring bulk power systems can greatly improve the adequacy of individual generating systems. In 1974, development of a multiple-area reliability program (PTI’s MAREL) helped solve some of the long-standing problems in this field of power system analysis. Efficient calculation of loss-of-load probability (LOLP) measures of capacity adequacy became possible for multiple interconnected areas in a manner which recognizes transmission transfer limitations between systems.1,2

MAREL has been used in several multi-area reliability studies since its development, some of which involve power systems encompassing areas as large as one or more NERC regions.4 One of these was the first comprehensive multi-area generation reliability study of various interconnections of ten utility systems in the Southwest portion of the U.S. Each system was represented as a distinct area, and the PTI MAREL program was used to compute the loss-of-load probabilities for the individual areas as well as for the total interconnection. This is the first reported bulk power reliability study in which more than three areas are interconnected without restrictions on the network configuration and with all area LOLP’s computed simultaneously.

The overall system studied consists of two major interconnected regional systems, each divided into a number of areas constituting one or more utility companies. The study was to perform a quantitative analysis of each area’s future generating-system adequacy, as measured by area LOLP values for alternative possible interconnection configurations. Total forecast peak load for the study system increases from about 55 GW in 1980 to 80 GW in 1980. Figure 1 shows the forecast transfer capabilities between areas in MW for the complete interconnected case for year 1980.

Four modes of regional interconnection were evaluated. Mode 1 uses areas 1, 2, 3, and 5 to form one system while areas 6 through 10 form another system which is not interconnected with the first. Note that area 4, rather remote from the others, is used for some sensitivity studies but not included in the interconnections. For Mode 2, areas 4, 7, 8, and 10 form one system while areas 6 and 9 are interconnected to the other areas. In Mode 3, area 10 is split into 10a and 10b with areas 7, 8, and 10a forming one system, and areas 6, 9, and 10b interconnected to the other areas. In Mode 4 all nine areas are interconnected.

In this study, a two-state model was used for all generating units, and the system of area interconnections was represented by a linear flow network in which the flow pattern was constrained by the network configuration and the capacity of the connecting links. The transfer capability of interconnections between areas was estimated conservatively to be equal to the sum of the surge impedance loadings of the individual transmission lines. Part of the purpose of this study was to determine the interconnection capability required to share generation reserves.

LOLP computations were performed for one year at a time, and each year was divided into three seasons. Generating unit maintenance was taken into account by adding the maintenance capacity out of service to the load even though the MAREL program has the option to model maintenance explicitly by leveling reserves. These load and maintenance representations were adequate for the study since this region is strongly summer peaking, and practically all the contribution to LOLP comes from the peak summer season during which little or no maintenance is carried out.

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DIGITAL DC SIMULATOR PROGRAM

The planning, design, and specification of dc transmission schemes require several levels of simulation capability. Overall functional requirements are normally studied with load flow and stability programs. This type of simulation permits evaluation of control and reactive compensation requirements and identifies other design measures which derive from fundamental frequency analysis. Figure 1 shows the modeling detail involved in fundamental frequency analysis. Dimensions of the PFI interactive program used for this purpose are 600 machines, 4000 buses, and 8000 lines (20 of which can be HVDC).1,2

Much more detailed modeling is required for the analysis of such other aspects of dc transmission as harmonics and filter behavior, rectifier and inverter commutation behavior during faults and voltage dips, performance with different types of reactive compensation (static capacitors, synchronous condensers, static var sources), and valve firing logic.

This detailed (transient) simulation has traditionally been done by analog methods; i.e., on special-purpose HVDC simulators. These simulators have been virtually indispensable in the practical introduction of HVDC, but they had the inherent limitations associated with any analog or physical "model" system; i.e., components have a restricted range of available characteristics, damping tends to be higher than for full-scale systems, and valve voltage drop is difficult to scale in proportion to other variables.

However, in August of 1976, PTI completed an intensive eighteen-month project to include detailed models of dc converters and dc transmission links in the Machine and Network Transients Program (MNT/E). MNT/E was originally developed for studies of subsynchronous oscillations in series capacitor compensated networks and their interaction with the dynamics of turbine-generator shafts.4 In the HVDC digital simulation, voltages, currents, control signals and valve firing logic are simulated on an instantaneous basis permitting the study of a wide range of harmonic and transient phenomena associated with dc conversion and transmission.

MNT/E treats both machines and 3-phase network in complete differential equation form, and accepts models of converters, dc lines, and inverters along with other ac system elements such as generators, transformers, lines, and reactive compensation (synchronous condensers, capacitors, filters, and static var sources)—all in complete, 3-phase form.

Figure 2 describes the modeling detail in MNT/E. The network voltages and currents are obtained from the solution of differential equations describing the 3-phase network characterized by lumped inductances, capacitances, and resistive elements.

The nonlinearities introduced by dc converters involve switching on and off of valves governed by voltage across valves and firing logic. Variations in firing logic can be readily incorporated within the modular structure of the program.

* MNT/E has also been used in simulations of load rejection transients where nonlinear effects of transformer and reactor saturation are of significance. This application was described in a previous Newsletter.3

FIGURE 1

FIGURE 2

The MNT/E program presently is capable of simulating the response of a system composed of up to 20 generators. Each generator can be modeled with two rotor circuits in each axis, with shaft torsional dynamics and respective turbines, governors, and excitation systems, if needed.

The network accommodates up to 50 3-phase buses and 100, 3-phase branches; 20 transformers with saturation representation; and 80 transmission lines represented by 3-phase sections. All network components may have unbalanced impedances and may be switched on an individual phase basis. Circuit breaker operation is automated, and upon command the phases open on individual current zeros.

The MNT/E program is operated in the interactive mode on PRIME 400 computers using a CRT console for dialog with the engineer. Computer-driven plotters provide a flexible output medium. Hard copy alphanumeric output is also possible. The computation can also be set up on batch mode for routine production of cases following exploratory phases of the study which are best accomplished in the interactive mode.

Figure 3 shows a sample dc transmission scheme with 12-pulse bi-pole converters and a parallel ac system. Figure 4 shows the normal performance of the system at 90% of full load. AC side voltages are shown along with dc voltage at the bi-pole and across one of the bridges. Currents through valves A and B are also displayed.

Figure 5 shows the A-phase voltage processed through a digital filter designed to cut off frequency components other than the 11th harmonic. The effect of disconnecting the 11th harmonic capacitor/inductor filter is shown. The filter currents going to zero show the instants of interruption of the filter phases. The resulting increase in harmonics on the voltage is also evident.

With an increasing trend in use of dc transmission throughout the world, the need for flexible simulator capability is expanding. The digital approach seems to offer a welcome alternative in filling this need.

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ARRAY PROCESSORS — A PROMISING NEWCOMER

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Array processors have recently received a lot of attention from specialists in power system network calculations. These relatively new and specialized digital computers appear to offer significant improvements in load flow, stability, and related power system calculations. PTI has purchased a Floating Point Systems AP120B array processor for attachment to one of its two Prime 400 computers. Initial development work will concentrate on its application in the PSS/E package. This article covers the general principles of the array processor. A forthcoming article will discuss array processor application and economics.

Computer Background

Conventional general-purpose digital computers are fundamentally serial-operating devices. A modern scientific computer like the Prime 400 has circuits for floating point multiplication, floating point addition, integer arithmetic, and so on; but it can only execute one of its many available arithmetic operations at a time. It waits until each operation is completed and its result can be tested before examining the next program instruction to determine what to do next. This fundamentally serial architecture of general-purpose digital computers has been, with refinement but no basic change, since the commercial introduction of digital computers in the 1950's.

We have become accustomed to continual improvements in speed and memory sizes in digital computers. These improvements, as far as the execution of computational algorithms is concerned, have occurred because of advances in circuit and memory components. Refinements of computer architecture have been a secondary factor in the advancement of load flow, stability, and related calculations.

Array processors, unlike successive generations of conventional computers, achieve a major increase in the speed of algorithm execution by exploiting a specialized architecture while using the same circuit and memory components as contemporary conventional computers.

While there are variations on the theme, array processors exploit two basic architectural features:

- parallel execution of multiple arithmetic operations, memory accesses, and branching logic
- "pipelined" construction of arithmetic units.

These terms deserve some explanation.

Array Processor Architecture

Figure 1 shows a very simplified array processor layout. The machine has separate units for floating point multiplication, floating point addition, and integer index arithmetic. It has several memories with differing access times and word lengths. These are used for storing floating point data, temporary results, and related calculations. The machine can initiate an operation of each of the three arithmetic units in parallel on every machine cycle. The program instruction tells the computer not what operation (add, multiply,
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store, etc.) is to be performed next, as in a conventional computer, but rather where the inputs to the arithmetic units are to come from and where their outputs are to go.

It is readily apparent that the multiplication operation initiated in a given machine cycle must be one that does not need the result of the addition that is initiated in parallel with it.

That the array processor can initiate a multiplication, addition, and index calculation in parallel every machine cycle is half the story. The second point is that this is done even though the add and multiply operations take two and three machine cycles, respectively, for their completion. To avoid frequent idle machine cycles, the addition and multiplication units are built as "pipelines." Their operation is illustrated in Figure 2. They execute each of their two or three sequential steps each machine cycle, with the result of each step being passed on immediately to the next. Three successive initiations are needed to push the result of the first initiation out of the end of the pipelines.

The advantage of pipelined processors becomes apparent when they are applied to repetitive computation sequences. Ten multiplications in a conventional computer would take 30 machine cycles. They would take the same 30 cycles in an array processor if the result of each were needed before the next could be initiated. If a pipelined multiplier can be presented with two prepared streams of multiplicands as shown in Figure 2, however, ten multiplications can be completed in 12 machine cycles. The effective multiply time of the pipelined unit is, therefore, 1.2 machine cycles rather than 3 cycles. Still further benefit can be obtained by feeding the result of one pipeline into the input of another. Hence ten multiply-and-add operations could be completed in 14 machine cycles with a pipelined multiplier feeding a pipelined adder, whereas a conventional computer would take 50 cycles for the same work.

Optimum use of the array processor requires the programmer to keep track of the delay between the initiation and completion of each particular arithmetic step of his algorithm and to find ways of exploiting the parallel/pipelined operation of the adder and multiplier. Consequently array processors are ill-suited to complex logical processes where the path through the program depends upon intermediate results, but are efficient in the execution of highly repetitive and logically simple algorithms.

REFERENCES

Reliability (continued from page 1)

MAREL computes two sets of area LOLP values simultaneously. The first assumes sharing of all generation capacity, and the second assumes the sharing of generation reserve capacity only. LOLP computations were performed for each of the four interconnection modes for one year of the study period. Results included area LOLP values for each of the four modes and values for isolated conditions. Several patterns of possible delay of units were also studied to assess the effects on the area reliabilities.

The MAREL program was also used to establish the inter-area transfer tie requirements for complete sharing of reserves between several of the areas. A series of reliability computations were performed, and plots of area LOLP values versus transfer capability into each respective area showed saturation of area LOLP values, indicating the optimum transfer requirements needed to achieve the near-minimum LOLP levels.

Multi-area generation reliability computation involves the evaluation of a very large number of possible system conditions and may possibly require a long computer time. Test studies on this large system containing over 400 units showed that computation time increased exponentially with the number of areas in the system and appeared excessive for studying the interconnection of the nine areas of Mode 4. A series of studies demonstrated that meaningful and conservative area LOLP results can be obtained at considerable savings in computing effort by limiting the number of load levels and capacity steps and using system equivalents. For the interconnected nine-area system shown in Figure 1, the equivalents used to compute area LOLP values consisted of first merging Areas 1, 2, 3, and 5 to compute the remaining area LOLP values and then merging Areas 6 through 10 and repeating the computation to determine the area LOLP values for the other four areas. The area LOLP values from these two computations agreed well with the corresponding values obtained from a nine-area study. Using the equivalents reduces the total computing time for the nine-area representation by 97 percent.

These studies provided valuable and meaningful results and also demonstrated the feasibility of multi-area computations for large interconnected systems. In addition to the preceding applications, the MAREL program may be used to study the benefits, scheduling, and selection of both generation and transmission capacity installations. The program has also been used to perform sensitivity studies of the effects on the generation system reliability due to changes in generation reserves, transfer capabilities, unit forced outage rates, and forecast loads.

REFERENCES